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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/874,173	GOLD ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 9/22/2004.

Drawings

3. The drawings are objected to because of the following minor informalities: Regarding Fig.2A, it is asked that applicant reposition four phrases on the right side of the figure such that they does not overlap the lines (wires). Doing so would increase clarity. Similarly, the wording in Fig.2B should also be repositioned so that it does not overlap the lines. Also, in Fig.3, applicant's wording should fit within each box. Therefore, the words in step 38 should be repositioned. Finally, in Fig.2A and Fig.2B, it is not clear what applicant is labeling with labels such as "free & soon-to-be free registers", "in-use, active registers", "in-use retired register", and "soon-to-be physical register numbers". Are these values on the wire connecting components 20 and 24 or are these values stored in the components themselves. Applicant should more clearly illustrate these figures. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the

appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Maintained Rejections

4. Except for claim 21, which was cancelled, applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and copied below for applicant's convenience.

35 USC § 112 Objections

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 1 is objected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, in the last paragraph of claim 1, it is not clear how an assignment of a register is assigned as a destination operand. Prior to the amendment, the register itself was assigned as the operand but now it appears as if applicant is claiming that an assignment (i.e.,

mapping or association of some type) is assigned as an operand. However, no data can be stored in an assignment. Instead, data is stored in a register. For purposes of this examination, the examiner will interpret the last paragraph of this claim as it appeared prior to the amendment, and also in a similar fashion to the other current independent claims.

Maintained Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-3, 5, 7-8, 10-12, 14, 17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Faraydon, EP Publication Number 0600611A2 (as disclosed by applicant, applied in the previous Office Action, and herein referred to as Faraydon).

9. Referring to claim 1, Faraydon has taught in a microprocessor having a plurality of physical registers, a method for managing said plurality of physical registers, said method comprising steps of:

a) providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor, said destination operand identifying where data resulting from an operation is to be stored. See Fig.6, and note the table made up of components 16 and 17. Each row corresponds to a different physical register and the lock bit for each register determines whether or not that particular register is free to be assigned as a destination operand. For instance, when the lock bit = 1, the

corresponding register is not free to be assigned as a destination for an instruction. However, when the lock bit = 0, the register is free.

b) storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. See Fig.8 and notice that CVT 0 is this second structure. More specifically, a physical register is assigned as a destination operand for the Add instruction. This is accomplished by setting the lock bit for register 04 in the first structure to a value of 1. Then, in the second structure (CVT 0), physical register 04 is assigned to logical register 03 (the destination of the Add instruction).

c) transferring said physical register assignment of said selected physical register from said second structure to a third structure after retirement of said selected instruction, the third structure holding information regarding a plurality of physical register assignments. See Fig.11 and Fig.12 and notice the communication between the second structure (CVT 0) and the third structure (Rename 2). When the instruction retires, the assignment is transferred from the second to third structure. That is, the mapping of register 03 to 04 in the second structure is transferred to the third structure. And the third structure (Rename 2) is able to hold up to 4 assignments.

d) when said selected physical register assignment of said selected physical register is assigned as a destination operand for a subsequent instruction, transferring information identifying said physical register as available to said first structure. When a subsequent instruction is assigned the selected physical register, the lock bit will be set in the first structure, thereby indicating that the selected register is made available to the subsequent instruction. In order to set this lock bit, a data value of 1 (information) must be transferred to the first structure. It should be realized that

applicant does not specify where this information is transferred from, nor what this information comprises.

10. Referring to claim 2, Faraydon has taught a method as described in claim 1. Faraydon has further taught storing mappings of logical registers to said plurality of physical registers. See the CVT tables and the Rename tables. Note that physical/logical mappings are stored in these tables. For instance, looking at Fig.13, in Rename 2, logical register 00 is assigned to physical register 00, logical register 01 is assigned to physical register 01, logical register 02 is assigned to physical register 02, and logical register 03 is assigned to physical register 04. The CVT tables hold similar mappings.

11. Referring to claim 3, Faraydon has taught a method as described in claim 2. Faraydon has further taught that the microprocessor is comprised of a memory array and wherein said method further comprises the step of storing said mappings to the memory array. From Fig.13, the mappings are stored in the CVT tables and the Rename tables. As can be seen from the figure, the CVT tables are shown as a 4x3 array (4 rows, 3 columns). Likewise, the Rename tables are essentially 4x1 arrays (4 rows, 1 column).

12. Referring to claim 5, Faraydon has taught a method as described in claim 1. Faraydon has further taught that contents of said first structure, second structure, and third structure of available registers are self-initialized to store mappings of said physical registers. See Fig.7, note that the physical registers in the first structure are mapped to lock bit values and actual data values. In the second structure, physical registers are mapped to flag values (000), which are changed as instructions are executed. See Fig.9, for instance, and note that the initial value of

000 has been changed to 100. Finally, the third structure (Rename 2) is initialized with mappings of physical to logical registers.

13. Referring to claim 7, Faraydon has taught a method as described in claim 1. Faraydon has further taught the step of detecting whether said assigned available physical registers are being utilized by said microprocessor for execution. If an available physical register is assigned to be a destination for an instruction, then that register is detected as being utilized during execution. That is, the processor will detect that register X is the destination and therefore, the result of the instruction will be written there.

14. Referring to claim 8, Faraydon has taught a method as described in claim 1. Faraydon has further taught that said method is performed by hardware. See Fig.2 and Fig.6+. Note that the method is performed by hardware.

15. Referring to claim 10, Faraydon has taught in a microprocessor having a plurality of physical registers, a method for managing said plurality of physical registers, said method comprising steps of:

a) providing a first structure for holding information identifying available physical registers that are free to be assigned to a plurality of destination operands for instructions executing on the microprocessor, said plurality of destination operands identifying where data resulting from an operation is to be stored. See Fig.6 and Fig.6+, and note the table made up of components 16 and 17. Each row corresponds to a different physical register and the lock bit for each register determines whether or not that particular register is free to be assigned as a destination operand. For instance, when the lock bit = 1, the corresponding register is not free to be assigned as a destination for an instruction. However, when the lock bit = 0, the register is free.

b) storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned to one of said plurality of destination operands for a selected instruction executing on the microprocessor. See Fig.8 and notice that CVT 0 is this second structure. More specifically, a physical register is assigned as a destination operand for the Add instruction. This is accomplished by setting the lock bit for register 04 in the first structure to a value of 1. Then, in the second structure (CVT 0), physical register 04 is assigned to logical register 03 (the destination of the Add instruction).

c) providing a third structure for holding information regarding available physical registers not utilized during execution of instructions. See Fig.8, and notice the "Rename 2" table. In this particular figure, this table specifies 4 physical registers (00-03). These registers are free since they have a lock bit of 0. And, registers 00 and 03 are not utilized during execution of the Add instruction (note that registers 01 and 02 are utilized as sources and 04 is used as the destination, not 03). Therefore, the third structure holds information regarding available registers not utilized during execution.

d) transferring said physical register assignment of said selected physical register from said second structure to said third structure after retirement of said selected instruction. See Fig.11 and Fig.12 and notice the communication between the second structure (CVT 0) and the third structure (Rename 2). When the instruction retires, the assignment is transferred from the second to third structure. That is, the mapping of register 03 to 04 in the second structure is transferred to the third structure.

e) and when said selected physical register is assigned as a destination operand for a subsequent instruction, transferring information identifying said selected physical register as available to

said first structure. When a subsequent instruction is assigned the selected physical register, the lock bit will be set in the first structure, thereby indicating that the selected register is made available to the subsequent instruction. In order to set this lock bit, a data value of 1 (information) must be transferred to the first structure. It should be realized that applicant does not specify where this information is transferred from, nor what this information comprises.

16. Referring to claim 11, Faraydon has taught a method as described in claim 10. Furthermore, claim 11 is rejected for the same reasons set forth in the rejection of claim 2 above.

17. Referring to claim 12, Faraydon has taught a method as described in claim 11. Furthermore, claim 12 is rejected for the same reasons set forth in the rejection of claim 3 above.

18. Referring to claim 14, Faraydon has taught a method as described in claim 10. Furthermore, claim 14 is rejected for the same reasons set forth in the rejection of claim 5 above.

19. Referring to claim 17, Faraydon has taught a method as described in claim 10. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8 above.

20. Referring to claim 19, Faraydon has taught a microprocessor system with a plurality of physical registers for managing a plurality of physical register assignments comprising:

a) a first module for providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor, said destination operand identifying where data resulting from an operation is to be stored. See Fig.6, and note the table made up of components 16 and 17. Each row corresponds to a different physical register and the lock bit for each register determines whether or not that particular register is free to be assigned as a destination operand. For

instance, when the lock bit = 1, the corresponding register is not free to be assigned as a destination for an instruction. However, when the lock bit = 0, the register is free.

b) a second module for storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. See Fig.8 and notice that CVT 0 is this second structure. More specifically, a physical register is assigned as a destination operand for the Add instruction. This is accomplished by setting the lock bit for register 04 in the first structure to a value of 1. Then, in the second structure (CVT 0), physical register 04 is assigned to logical register 03 (the destination of the Add instruction).

c) a third module for providing a third structure for holding information regarding available physical registers not utilized during execution of instructions. See Fig.8, and notice the "Rename 2" table. In this particular figure, this table specifies 4 physical registers (00-03). These registers are free since they have a lock bit of 0. And, registers 00 and 03 are not utilized during execution of the Add instruction (note that registers 01 and 02 are utilized as sources and 04 is used as the destination, not 03). Therefore, the third structure holds information regarding available registers not utilized during execution.

d) a first interface for transferring said physical register assignment of said selected physical register from said second structure to said third structure after retirement of said selected instruction. See Fig.11 and Fig.12 and notice the communication between the second structure (CVT 0) and the third structure (Rename 2). When the instruction retires, the assignment is transferred from the second to third structure. That is, the mapping of register 03 to 04 in the second structure is transferred to the third structure.

e) a second interface for, when said selected physical register is assigned as a destination operand for a subsequent instruction, transferring information identifying said selected physical register as available to said first structure. When a subsequent instruction is assigned the selected physical register, the lock bit will be set in the first structure, thereby indicating that the selected register is made available to the subsequent instruction. In order to set this lock bit, a data value of 1 (information) must be transferred to the first structure. It should be realized that applicant does not specify where this information is transferred from, nor what this information comprises.

Maintained Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 4, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraydon, as applied above.

23. Referring to claim 4, Faraydon has taught a method as described in claim 1. Faraydon has not taught that said microprocessor simultaneously executes multiple threads. However, Official Notice is taken that threads and the ability of a processor to execute multiple threads in parallel (simultaneously) is well known and expected in the art. Threads are separate independent sections of code which perform a particular task. They are advantageous in that they hide the latency of a processor while performing a long-latency instruction such as a load from main memory. Instead of simply stalling and waiting for the result, the processor can

switch to another thread and continue executing. In addition, when threads are executed in parallel, more work is being performed in a given amount of time, compared with executing a single thread at a time, serially. As a result, in order to increase the efficiency of the system, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Faraydon to execute multiple threads simultaneously.

24. Referring to claim 13, Faraydon has taught a method as described in claim 10. Furthermore, claim 13 is rejected for the same reasons set forth in the rejection of claim 4 above.

25. Referring to claim 20, Faraydon has taught a method as described in claim 19. Furthermore, claim 20 is rejected for the same reasons set forth in the rejection of claim 4 above.

26. Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraydon, as applied above, in view of Yung et al., U.S. Patent No. 5,546,554 (as disclosed by applicant, applied in the previous Office Action, and herein referred to as Yung).

27. Referring to claim 6, Faraydon has taught a method as described in claim 1. Faraydon has not taught that contents of said assigned available physical registers are flushed from said assigned available physical registers. However, Yung has taught such a concept. See column 12, line 26, to column 13, line 5, and Fig.13b, 14b, and 15b. Note that if an instruction causes an exception, it along with all of the younger instructions must be flushed, including their results, so that the system can be restored to the state prior to the exception. If this flushing does not occur, then the system will contain corrupt/incorrect data which would cause the program to yield incorrect results. Consequently, it would have been obvious to one of ordinary skill in the art at

the time of the invention to modify Faraydon in view of Yung such that contents of assigned physical registers in Faraydon are flushed when exceptions occur.

28. Referring to claim 15, Faraydon has taught a method as described in claim 10. Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 6 above.

29. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraydon, as applied above, in view of Tanenbaum, Structured Computer Organization, 2nd Edition, 1984, page 11 (as applied in the previous Office Action and herein referred to as Tanenbaum).

30. Referring to claim 18, Faraydon has taught a method as described in claim 1. Although Faraydon has taught that said method is performed by hardware (Fig.2 and Fig.6+), Faraydon has not explicitly taught that said method is performed by software. However, Tanenbaum has taught that hardware and software are logically equivalent. See page 11. Therefore, a person of ordinary skill in the art would've recognized that the function performed by the hardware could be implemented in software and vice-versa. As Tanenbaum has further suggested, the choice between hardware and software implementations is based on the designer's needs as well as cost, speed, reliability, and frequency. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Faraydon such that software performs the method instead of hardware.

31. Referring to claim 18, Faraydon has taught a method as described in claim 10. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9 above.

Response to Arguments

32. Applicant's arguments filed on September 22, 2004, have been fully considered but they are not persuasive.

33. Applicant argues the novelty/rejection of claim 1 on page 15 of the remarks, in substance that:

> "In contrast, to the Faraydon reference, Claim 1 recites a step of providing a first structure holding information identifying available physical registers that are free to be assigned as destination operand for instructions executing on the microprocessor. Claim 1 further recites a step of storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. The Faraydon reference does not disclose such features. The Faraydon reference discloses one structure, a CVT table to hold information identifying physical registers free to be assigned as destination operand for instructions executing on the microprocessor (i.e., first column of a CVT table) and a physical register assignment (i.e., second column of the CVT table) and a note indicating the selected physical register is assigned as a destination operand for a selected instruction (i.e., third column of the CVT table). The Faraydon reference does not anticipate Claim 1.
>
> The Examiner submits that the general purpose registers (GPR)(16) and the associated lock bits (17) disclosed by Faraydon correspond to the first structure of Claim 1. Applicants respectfully disagree. To the contrary, the lock bits associated with the physical locations of general purpose registers (16) disclosed by Faraydon do not identify available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. Rather, the lock bits of Faraydon are used to prevent the reading or writing to physical registers before an instruction has retired to ensure proper data dependencies. For example, as shown in Figure 8 of Faraydon, the first four registers (00-03) of the illustrated GPR each have a lock bit value of (0) and the fifth register (04) has a lock bit value of (1). Nevertheless, the second register (01) and the third register (02), which are source registers that hold data for an instruction and are not free to be assigned as a destination operand for instructions executing on the microprocessor. Hence, following the Examiner's assertions then a lock bit of value (0) indicates a free register available as a destination of an operand leaving source registers (01) and (02) available as destinations for an operand. Furthermore, the Faraydon reference discloses that the lock bits are used to control dependencies between source registers and destination registers and are not meant to indicate an available physical register. That function in the Faraydon reference is carried out by the CVT table. Accordingly, the Faraydon reference does not anticipate Claim 1."

34. These arguments are not found persuasive for the following reasons:

a) It is asserted that applicant is reading the claim too narrowly. The examiner maintains the position that the lock bits within the first structure (components 16 and 17) may be read as information which represents free registers. The examiner agrees with applicant that the lock

bits are used for either allowing or preventing reading and writing to associated registers. However, in doing so, they also dictate which registers are free for assignment. More specifically, when a register is allocated to an instruction, the associated lock bit changes from 0 to 1, and it will stay 1 until the result is written to that register. At this point, the lock bit will return to 0. Consequently, as long as a given register has a lock bit of 1, that register is locked and not free (no instruction can access it). On the other hand, those with lock bits of 0 are unlocked or free (instructions may access it and it may be used for allocation purposes). To summarize, the registers are either in a locked or unlocked state. Only when they are in an unlocked state may they be allocated to an instruction. The examiner has not stated that all registers with a lock bit of 0 will be assigned. However, only registers with a lock bit of 0 can be assigned, as they clearly cannot be assigned when they have a lock bit of 1, and therefore, this is an indicator of "freeness" (the only registers that will be allocated will have a lock bit = 0). In addition, even if the CVT table helps in the determination of which register to assign, the first structure still hold the information (lock bits) which represents the "freeness" of the registers and this is enough to read on the claim.

Similar arguments have been made for claims 10 and 19 and consequently, the arguments against the rejections of those claims are responded to in the same fashion as above.

35. Applicant argues the novelty/rejection of claim 4 on page 22 of the remarks, in substance that:

> "Applicants' traverse the Examiner's assertion of Official Notice that a microprocessor simultaneously executes multiple threads at the time the invention was made was well known. In support of Applicants' assertion that a microprocessor simultaneously executes multiple threads at the time the invention was made was well known Applicants' contend that the Examiner's reasoning regarding the amount of work that can be performed in parallel versus a single thread.

> That is, one skilled in the art would recognize that in a multi-thread mode the number of available registers in the processor is shared amongst all of the threads, hence limiting the amount of work do to resource contention. However, in a single thread mode, all available registers can be allocated to the one thread avoiding resource contention and in fact increasing the amount of work the processor can handle. Hence, the Examiner's reasoning underlying the decision to take such notice is unclear and flawed. Hence, Applicants' specifically point out why the noticed fact is not considered to be common knowledge or well known in the art, and further request the Examiner to submit documentary evidence in support of such a finding in any further rejection taken under Official Notice."

36. These arguments are not found persuasive for the following reasons:

a) In response to applicant's request to receive evidence in support of the examiner's Official Notice, the examiner provides Eggers et al., "Simultaneous Multithreading: A Platform for Next-generation Processors," 1997. On pages 2-3 of Eggers, Fig.1a,b,c and their descriptions should be noted. Note from Fig.1a, a single thread executes. It is common, due to dependencies or other latency events, the maximum amount of instructions (or any instruction at all) are unable to be issued every cycle. If this is the case, then wasteful processing is achieved. However, if multiple threads may be executed in parallel such as in Fig.1b and Fig.1c, less waste is achieved and therefore, more work may be performed. For instance, Fig.1b shows that when one thread can't continue due to a stall, another thread is switched in. This is one interpretation of threads executing in parallel because even though different threads are not explicitly executed every cycle, the overall execution of the threads is done in parallel. On the other hand, Fig.1c shows an even more obvious version of parallel thread processing where different threads are executed together each cycle. As can be seen, much less waste is achieved, thereby allowing more work to be performed. From this evidence, the examiner asserts that the Official Notice was not flawed or unclear. Consequently, the examiner maintains the obvious-type rejection of claim 4.

Similar arguments have been made for claims 13 and 20 and consequently, the arguments against the rejections of those claims are responded to in the same fashion as above.

37. Applicant argues the novelty/rejection of claim 6 on page 25 of the remarks, in substance that:

> "Yung is cited for teaching or suggesting that the contents of the assigned available physical registers are flushed from the assigned available physical registers. Nevertheless, the Yung reference fails to bridge the factual deficiencies of the Faraydon reference. That is, the Yung reference does not disclose a method for managing a number of physical registers in a microprocessor having a plurality of physical registers as recited in Claim 1. Accordingly, neither Yung nor Faraydon, alone or in combination, detract from the patentability of Claim 6."

38. These arguments are not found persuasive for the following reasons:

a) Based on the examiner's response to applicant's arguments regarding claim 1 above, it is asserted that Faraydon does not include factual deficiencies and therefore, Yung is not required to teach such deficiencies.

Similar arguments have been made for claims 9, 15, and 18, and consequently, the arguments against the rejections of those claims are responded to in the same fashion as above.

Conclusion

39. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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November 2, 2004

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